REMARKS

Claims 1-7 were originally filed. Claim 8 was added by a previous amendment. Claims 1-8 are rejected in the Office Action. Claims 1-8 are pending.

In the Office Action claims 1-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,862,354 to Curiger, et al., in view of U.S. Patent No. 5,412,072 B2 to Little, et al., and further in view of U.S. Patent No. 5,898,859 to Kardach, et al.

Per claims 1-4:

Claim 1 requires, among other things: a data direction switch for directing the flow of data between said primary one-wire bus and said secondary one-wire bus. Applicant respectfully submits that none of the cited references disclose a data direction switch which directs the flow of data between multiple busses. The test interface circuitry and timed access circuitry of Little, et al., simply require a processor to perform correct data writes at correct addresses within particular timing constraints before the processor is free to write to memory. Essentially an unlocking scheme, this protects the memory from accidental writes in the event of a runaway processor (Col. 6, lines 18-30, Col. 16, lines 25-54). This scheme does not involve the switching of data between discrete busses. There is no disclosure of directing data flow between two distinct busses.

Kardach, et al., provides a scheme for emulating a slave device through a shadow register. Kardach, et al., does not provide data switching between separate busses, but instead, upon receiving a shadow address match on one bus 150, may access an emulated device through a signal line 138 and an interrupt routine triggered by the match at the shadow register. Data is never switched so as

to pass directly between bus 150 and a second bus (Col. 5, lines 1-9, Col. 4, lines 4-12). The emulated device is accessed without resorting to the first bus 150, at all. (Col. 8 lines 15-16). Claim 1 requires data flow between the primary one-wire bus and the secondary one-wire bus, thus both busses are involved in the communication. None of the references cited in the Office Action disclose such a data path.

It should be noted that claim 2 has been amended to clarify that the antecedent for --translator— is indeed the translator device.

Applicant thus submits that claim 1 is in condition for allowance. Claims 2-4 depend from claim 1 and, at least for the reasons stated with regard to claim 1, are likewise in condition for allowance. Reconsideration and allowance of claims 1-4 are respectfully requested.

Per claim 5:

Claim 5 has been amended to clarify the operation of the enhanced one wire bus in that there is an operational mode of the bus, the third mode, wherein a potion of a message from the slave on the secondary one wire bus is modified as the message is passed along to the master on the primary one wire bus. This limitation is not present in any of the cited references. This operation is described in the specification at page 19, line 13 through page 20, line 13.

Applicant thus submits that claim 5 is in condition for allowance. Reexamination and allowance of claim 5 are respectfully requested.

Per claim 6:

As an initial matter, it should be noted that Applicant's use of the word "interruptible" is in

a different context, and has a different meaning, than the word "interrupt" as used in the cited references. As quoted in the Office Action, "interrupt" is used along with the term "vector" and "routine" which clearly indicates that term is used to describe exception processing within the microcomputer. This exception processing, or interrupt processing, involves the vectoring of the program counter to an interrupt, or exception, routine in response to an external or internal stimulus. Absent further disclosure, this does not indicate that the transmission of data which resulted in the vectoring is in some way interruptible. In contrast, the term "interruptible" is used in the present application to indicate that the data stream itself can be disrupted. Thus, "interrupt" as sued in the cited reference is a noun used to describe a particular type of software process while in the present application it is used as a verb to describe the act of disrupting the normal flow of data on the bus.

Applicant respectfully submits that none of the cited references discuss interrupting data flowing between two busses to insert known data into the data stream as required by claim 6. Applicant thus submits that claim 6 is in condition for allowance. Reconsideration and allowance of claim 6 are respectfully requested.

Per claim 7:

It should be noted that claim 7 has been amended to clarify the relationship between certain identifiers and predetermined data, and to correct an ambiguity with respect to which one-wire bus is used for the transmission of step (g). Claim 7 has also been amended to clarify that communications in the process are viewed from the perspective of the translator device.

While several differences exist between the process of claim 7 and the processes disclosed

in the cited references, one noteworthy difference that, with regard to ROM commands, the translator performs the processes normally undertaken by the slave device. With respect to memory commands, the slave device performs its normal processes. There is no disclosure of a like process in the cited references wherein emulation, and/or simulation, occurs selectively relative to the type of command.

Applicant thus submits that claim 7 is in condition for allowance. Reexamination and allowance of claim 7 are respectfully requested.

Per claim 8:

Like claim 1, claim 8 requires, among other things: a data direction switch for directing the flow of data between said primary one-wire bus and said secondary one-wire bus. As discussed with regard to claim 1, Applicant respectfully submits that none of the cited references disclose a data direction switch which directs the flow of data between multiple busses. The test interface circuitry and timed access circuitry of Little, et al., simply provides an unlocking scheme to protect memory from accidental write operations and does not involve the switching of data between discrete busses. There is no disclosure of directing data flow between two distinct busses.

Kardach, et al., provides a scheme for emulating a slave device through a shadow register and does not provide data switching between separate busses. Data is never switched so as to pass directly between busses. Claim 8 requires data flow between the primary one-wire bus and the secondary one-wire bus, thus both busses are involved in the communication. None of the references cited in the Office Action disclose such a data path.

Applicant thus submits that claim 8 is in condition for allowance. Reconsideration and allowance of claim 8 are respectfully requested.

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This paper is intended to constitute a complete response to the outstanding Office Action. Please contact the undersigned if it appears that a portion of this response is missing or if there remain any additional matters to resolve. If the Examiner feels that processing of the application can be expedited in any respect by a personal conference, please consider this an invitation to contact the undersigned by phone.

Respectfully submitted,

Date: July 21, 2005

SIGNATURE OF PRACTITIONER

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